## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device for refreshing data stored in a memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells wherein the N number of unit cell blocks are corresponded to logical cell block addresses and one unit cell block is added for accessing data with high speed;

a predetermined cell block table for assigning M number of word lines among the (N+1) x M number of the word lines as predetermined restorable word lines;

a tag block having N+1 number of unit tag blocks, each unit tag block storing at least one physical cell block address storing data wherein the tag block receives a logical cell block address designated for accessing one of N number of unit cell blocks and converts the logical cell block address into a physical cell block address designated for accessing one of the N+1 number of unit cell blocks; and

a control means for activating one word line of a unit cell block selected by the physical cell block address and a corresponding one of the predetermined restorable word lines by controlling the tag block and ~~a~~ the predetermined cell block table ~~for refreshing the data in the plurality of unit cells coupled to a word line in response to at least one physical cell block address~~,

wherein the tag block stores information representing an update of the logical cell block address ~~the converted physical cell block address~~ and a refresh operation is preformed through the use of the information.

2. (Currently Amended) The semiconductor device as recited in claim 1, ~~further comprising:~~

~~a predetermined cell block table for storing information representing at least more than one word line among the M number of the word lines storing data.~~

wherein the corresponding one of the predetermined restorable word lines is located at a

unit cell block except for the unit cell block selected by the physical cell block address.

3. (Currently Amended) The semiconductor memory device as recited in claim 1, wherein the tag block includes:

an N+1 number of unit tag tables corresponded to the N+1 unit cell blocks, each unit tag table having M number of registers for storing the at least one physical cell block address denoting a row address storing data;

~~a~~ an N+1 number of comparators corresponded to the N+1 number of unit tag blocks, each comparator for comparing address information stored in registers of the corresponding unit tag table with a logical cell block address sensed by the row address wherein the address information is the at least one physical cell block address denoting the row address storing the data;

~~a~~ an encoder for outputting the at least one physical cell block address by encoding results compared by the N+1 number of comparators; and

a tag control block for controlling the N+1 number of the unit tag tables, the N+1 number of the comparators, and the encoder.

4. (Currently Amended) The semiconductor memory device as recited in claim 3, wherein each register of a unit tag table includes:

a first register having X bits for storing the logical cell block address representing a unit cell block, wherein X is at least $\log_2 N$ ; and

a second register for storing ~~the~~ information representing an update of data stored in the first register.

5. (Previously Amended) The semiconductor memory device as recited in claim 3, wherein the tag block further includes:

a decoder for receiving candidate information and outputting the logical cell block address.

6. (Currently Amended) The semiconductor memory device as recited in claim 4,

wherein the predetermined cell block table includes M number of third registers for storing information indicating which word lines of (N + 1) x M ~~(N+1) * M~~ word lines included in the N+1 number of the physical unit cell blocks are the M number of the predetermined restorable word lines, each third register having X+1 bits.

7. (Currently Amended) A method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a predetermined cell block table for assigning M number of word lines among (N + 1) x M number of the word lines as predetermined restorable word lines; and a tag block for storing a physical cell block address, the tag block having N+1 number of unit tag blocks, each having M number of registers for sensing an update of data, wherein one word line of a unit cell block selected by the physical cell block address and a corresponding one of the predetermined restorable word lines are activated, comprising the steps of:

(A) starting a refresh mode ~~in response to refresh signal~~;

(B) detecting ~~at least one physical cell block address and~~ word ~~line~~ lines determined by the physical cell block address having data by checking (N + 1) x M ~~(N+1)×M~~ number of registers in the tag block, each register storing a logical block address and an information representing update of the logical block address; and

(C) performing the refresh operation through the use of the information,

wherein the N number of unit cell blocks are corresponded to addresses and one unit cell block is added for accessing data with high speed.

8. (Currently Amended) The method as recited in claim 7, wherein the step (C), includes the step of

(D) denoting M number of registers in ~~a~~ the predetermined cell block table in order to find out an address representing the M number of predetermined restorable word lines assigned among (N + 1) x M ~~(N+1) * M~~ word lines of the N+1 number of unit cell blocks,

wherein the refresh operation is performed except for the address representing the M

number of the predetermined restorable word lines.

9. (New) The method as recited in claim 7, wherein the corresponding one of the predetermined restorable word lines is located at a unit cell block except for the unit cell block selected by the physical cell block address.

10. (New) The method as recited in claim 9, wherein the information represents which one of two activated word lines has real data.

11. (New) The method as recited in claim 10, wherein in the step (C), the refresh operation is only performed to the word line having the real data.

12. (New) The semiconductor device as recited in claim 1, wherein the information represents which one of two activated word lines has real data.